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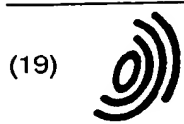
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(71) Applicant:
ALCATEL STANDARD ELECTRICA, S.A.
28045 Madrid (ES)

(72) Inventor:
Alvarez Alvarez, Manuel José
E-28820 Coslada (Madrid) (ES)

(74) Representative:
Fera, Valérie et al
Alcatel Espana S.A.
Patent Department
Ramirez de Prado 5
28045 Madrid (ES)

(54) Device for implementation of DECT encryption algorithm with reduced current consumption

(57) The invention has application to the implementation of the DECT standard data ciphering algorithm which requires a lengthy procedure of key loading and logic operations during the stages of pre-ciphering and ciphering and requiring clocks operating at different frequencies.

This device performs parallel mode loading of the shift registers, with a ciphering keyword. It also calculates, in a first cycle, during the pre-ciphering, the values of the bits of each shift register that determine the value of the next shift in order to, in a second cycle, effect parallel mode shifting in these registers with a value equal to the sum of the two previous shift values.

During the ciphering process, the shifting is done in the registers, in parallel mode and in a single data clock cycle, with a value equivalent to the serial value obtained by the algorithm.

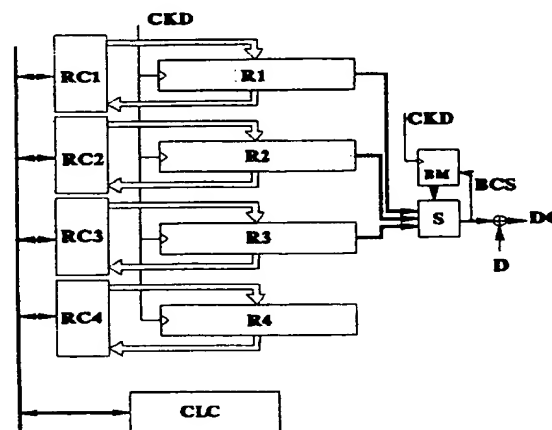


FIG. 5

EP 0 661 843 A3



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 94 11 9371

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DOCUMENTS CONSIDERED TO BE RELEVANT			
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			H04L
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	15 September 1999	HOLPER, G	
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EP 94 11 9371

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15-09-1999

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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